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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,540	01/29/2004	Mirmira Ramarao Dwarakanath	ENP-003	5353

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EXAMINER	
BEHM, HARRY RAYMOND	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 09/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,540	DWARAKANATH ET AL.	
	Examiner	Art Unit	
	Harry Behm	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-20 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-20 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 16-20 and 24-30 in the reply received 8/18/06 is acknowledged.

Drawings

The drawings were received on 6/02/06. These drawings are accepted.

Response to Arguments

Applicant's arguments, see page 11, filed 6/02/06, with respect to the rejection(s) of claim(s) 1-24 under 35 USC 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Capici (US 6,477,065).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-20 and 24-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Capici (US 6,320,449).

With respect to Claim 16, Capici discloses a power converter (Fig. 5 1) couplable to a source of electrical power (Fig. 5 VAL) adapted to provide an input voltage thereto, comprising: a power train including a switch (Fig. 5 2), referenced to said input voltage (Fig. 5 VAL) and subject to a control voltage limit [MOS PCHANNEL has control voltage

limit], configured to conduct for a duty cycle (duty cycle of GATE) and provide a regulated output characteristic at an output of said power converter (Fig. 5 VOUT); a controller (Fig. 5 5) configured to provide a signal (Fig. 5 ON/OFF) to control said duty cycle of said switch (Fig. 5 2); and a driver (Fig. 5 4,7,8,3) including switching circuitry (Fig. 5 4,7) referenced to a voltage level [7 is referenced to GATE voltage G, 4 is referenced to the voltage of the current source] different from said input voltage (Fig. 5 VAL) and configured to provide a drive signal (Fig. 5 GATE) for said switch within said control voltage limit [MOS PCHANNEL is not damaged] as a function of said signal from said controller.

With respect to Claim 17, Capici discloses the power converter as recited in claim 16 wherein said controller is configured to provide a complement (Fig. 5 ON and OFF) of said signal to control said duty cycle of said switch, said driver being configured to provide said drive signal for said switch within said control voltage limit as a function of said complement of said signal from said controller.

With respect to Claim 18, Capici discloses the power converter as recited in claim 16 wherein said switch is a metal oxide semiconductor field effect transistor (Fig. 5 2 MOS PCHANNEL) (MOSFET) referenced to said input voltage (Fig. 5 VAL), said switching circuitry (Fig. 5 7,4) configured to provide a gate drive signal (Fig. 5 GATE) for said switch within a gate voltage limit thereof.

With respect to Claim 19, Capici discloses the power converter as recited in claim 16 (Fig. 9 is a more detailed schematic) wherein said switching circuitry comprises a plurality of driver switches (Fig. 9 M1,M6,X2,transistor between M1-M2) couplable to

ground (Fig. 9 gnd), ones (Fig. 9 transistor between M1-M2)of said plurality of driver switches (Fig. 5 4) being couplable to said ground (Fig. 9 gnd), said source of electrical power (Fig. 9 VAL) and a bias voltage source (Fig. 9 VBIAS) for providing a bias voltage, ones (Fig. 9 M5)of said plurality of driver switches configured to cooperate to provide said drive signal (Fig. 9 GATE POWER) referenced to said input voltage (Fig. 9 VAL) and within said control voltage limit of said switch.

With respect to Claim 20, Capici discloses the power converter as recited in claim 16 wherein said switching circuitry comprises at least one driver switch configured to enable a mode of operation [normal operation] wherein said drive signal (Fig. 7 GATE) for said switch is referenced to said voltage level [gate voltage at time T4].

With respect to Claim 24, Capici discloses the power converter as recited in Claim 16 wherein a voltage of said drive signal (Fig. 7 GATE) is less than said input voltage (Fig. 7 GATE at time T4).

With respect to Claim 25, Capici discloses a method of operating a converter (Fig. 9 1) couplable to a source of electrical power (Fig. 9 VAL) adapted to provide an input voltage thereto, comprising controlling a power train including a switch (Fig. 9 2), referenced to said input voltage and subject to a control voltage limit [since power switch is not damaged in operation, it is subject to a control voltage limit], to conduct for a duty cycle [switching power supply] and provide a regulated output characteristic (Fig. 9 Vout) at an output of said power converter; providing a signal (Fig. 9 ON) to control said duty cycle of said switch; and providing a drive signal (Fig. 9 GATE_POWER) for said switch within said control voltage limit as a function of said signal with a driver

including switching circuitry referenced to a voltage level different form said input voltage.

With respect to Claim 26, Capici discloses the method as recited in Claim 25, further comprising: providing a complement (Fig. 9 OFF) of said signal to control said duty cycle of said switch; and providing said drive signal (Fig. 9 GATE_POWER) for said switch within said control voltage limit as a function of said complement of said signal.

With respect to Claim 27, Capici discloses the method as recited in claim 25 wherein said switch is a metal oxide semiconductor field effect (Fig. 9 2) transistor (MOSFET) referenced to said input voltage (Fig. 9 VAL), said drive signal (Fig. 9 GATE_POWER) being a gate drive signal for said switch within a gate voltage limit thereof.

With respect to Claim 28, Capici discloses the method as recited in claim 25 wherein said switching circuitry comprises a plurality of driver switches (Fig. 9 M1,X2,M6,transistor between M1-M2), ones (Fig. 9 transistor between M1-M2) of said plurality of driver switches being couplable to said ground (Fig. 9 gnd), said source of electrical power (Fig. 9 VAL) and a bias voltage (Fig. 9 VBIAS) source for providing a bias voltage, ones (Fig. 9 M6) of said plurality of driver switches configured to cooperate to provide said drive signal referenced to said input voltage (Fig. 9 VAL) and within said control voltage limit of said switch.

With respect to Claim 29, Capici discloses the method as recited in claim 25 further comprising a mode of operation [normal operation] wherein said drive signal

(Fig. 9 GATE_POWER) for said switch is referenced to said voltage level (Fig. 7 voltage time T4).

With respect to Claim 30, Capici discloses the method as recited in claim 25 wherein a voltage of said drive signal (Fig. 9 GATE_POWER) is less than said input voltage (Fig. 9 VAL).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional 35 USC 102 rejections could be made with the following references: Jacobs (US 6,822,882), Faye (US 6,650,169) Pulkin (US 6,573,694), Parks (US 6,477,065), Kashimoto (US 6,262,564), Kanakmori (US 6,262,564) and Li (US 6,388,468) disclose drivers including switching circuitry referenced to a voltage level different from the input voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on Business EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-2721989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KARL EASTHOM
SUPERVISORY PATENT EXAMINER